IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application No.: 10/027,359
Filed: December 19, 2001
Inventor:
Fay Chong, Jr.

Title: Cache Accumulator Memory for Performing Operations on Block Operands

Examiner: Tsai, Sheng Jen
Group/Art Unit: 2186
Atty. Dkt. No: 5681-05200

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Robert C. Kowert
Name of Registered Representative

Signature

February 7, 2006
Date

PRE-APPEAL BRIEF REQUEST FOR REVIEW

Mail Stop AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Applicant requests review of the rejection of claims 2-9, 11-15, 17-26 and 28-34 in the Final Action of November 28, 2005 in the above-identified application. No amendments are being filed with this request. This request is being filed with a notice of appeal. The review is requested for the reasons stated below.

Claims 2-9, 11-15, 17-26 and 28-34 remain pending in the application. Reconsideration of the present case is earnestly requested in light of the following remarks. Please note that for brevity, only the primary arguments directed to the independent claims and selected dependent claims are presented, and that additional arguments, e.g., directed to the subject matter of the remaining dependent claims, will be presented if and when the case proceeds to Appeal.

Claims 4-6, 9, 11-15, 17, 20, 23-26 and 28-34 are rejected under 35 U.S.C. § 102(b) as being anticipated by Crater et al. (U.S. Patent 5,146,588) (hereinafter "Crater"). Various

dependent claims are rejected under 35 U.S.C. § 103(a) as indicated in the Office Action. The following clear errors in the Examiner's rejection are noted.

Crater fails to teach or suggest all of the limitations of Applicant's claim 32. Specifically, Crater fails to teach or suggest an apparatus including a storage array including a plurality of mass storage devices, as well as an array controller configured to perform block operations on data stored to the storage array; wherein the array controller includes a cache accumulator memory configured as a cache of a memory and a functional unit configured to perform a block operation on one or more block operands to generate a block result; and wherein in response to an instruction using an address in the memory to identify a first block operand, the cache accumulator memory is configured to output the first block operand to the functional unit and to accumulate an intermediate result of a block accumulation operation performed on the first block operand, wherein the intermediate result is both a result of and an operand of the block accumulation operation.

In rejecting claim 1, the Examiner asserts that the redundancy accumulator 301 of Crater corresponds to Applicant's claimed cache accumulator memory, and that Crater's inclusion of redundancy accumulator 301 within a unit denoted as "cache 113" is a disclosure of Applicant's recitation that the cache accumulator memory is a cache of a memory. However, the Examiner's assertion is not supported by the structure disclosed by Crater. Although Crater discloses cache 113, Crater does not describe in any way that redundancy accumulator 301 is itself configured as a cache of any memory. Crater describes the function of redundancy accumulator 301 as simply to temporarily "...store the intermediate result of ... redundancy calculations until all of the physical tracks have been included in the redundancy calculation." (col. 7, lines 55-57). Crater does not disclose any relationship between the contents of redundancy accumulator 301 and other data storage elements within cache 113, much less a caching relationship as recited in Applicant's claim.

The Examiner seems to imply that because Crater's redundancy accumulator 301 is included within a cache, redundancy accumulator 301 must itself function as a cache. This simply does not follow. Crater discloses that cache 113 functions as a cache with respect to data transfers between host processors 11, 12 and disk drive subsets 103 (FIG. 1 and col. 6, lines 7-12, 38-39). This operation occurs at an entirely different level of scope than the relationship between cache 113 and its component, redundancy accumulator 301. That is, the fact that cache 113

functions as a cache with respect to host processors 11, 12 and disk drive subsets 103 does not entail that redundancy accumulator 301 functions as a cache with respect to cache 113 or anything else, and in fact Crater discloses no such relationship.

In responding to the above remarks in the Final Action, the Examiner asserts that (1) Crater discloses a redundancy accumulator to be included within a cache memory controller, (2) the cache memory of Crater functions as a cache between storage devices and host processors, and (3) data transfers between a host and a redundancy subgroup of disk drives of Crater must pass through the redundancy accumulator. However, Applicant fails to see how these remarks bear on the arguments made above with respect to the limitations of claim 32. Specifically, the fact that Crater includes a cache that itself includes a redundancy accumulator does not entail that Crater discloses the recited cache accumulator memory – **a *single entity* that is configured both as a cache of a memory and an accumulator for a block accumulation operation**, which is included within an array controller along with a function unit configured to perform the block accumulation operation As the Examiner notes, Crater discloses that redundancy accumulator 301 is included within cache memory controllers 331, 332, which are entirely distinct from the memory elements 340-355 that actually store data within cache 301.

Thus, as argued above, Crater does not disclose how redundancy accumulator 301 also functions as a cache, as required by Applicant's claim. **Mere inclusion of a given element within something generally denoted as a "cache" does not on that basis alone render *the given element* a cache.** The Examiner's remarks as to the path of data flow through cache 113 and redundancy accumulator 301 do not entail that redundancy accumulator 301 is itself a cache; again, as described above, Crater ascribes the storage functionality of cache 113 to a set of elements completely distinct from redundancy accumulator 301.

Applicant notes that anticipation requires the presence in a single prior art reference disclosure of each and every element of the claimed invention, arranged as in the claim. M.P.E.P 2131; *Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co.*, 221 USPQ 481, 485 (Fed. Cir. 1984). The identical invention must be shown in as complete detail as is contained in the claims. *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). The teachings of Crater clearly do not disclose the arrangement of elements recited in claim 32. A similar argument applies to independent claims 28, 33 and 34, which recite limitations similar to

those of claim 1. Applicant therefore submits that each of these claims is not anticipated by Crater.

Crater further fails to teach or suggest all of the limitations recited in Applicant's claim 5. Specifically, Crater does not teach or suggest that the cache accumulator memory is configured to load a copy of the block operand into the cache accumulator memory from the memory in response to the block operand not being present in the cache accumulator memory when the instruction is received. In rejecting claim 5, the Examiner asserts that in Crater, the first block operand is loaded into redundancy accumulator 301 from the disk drives via the DATA INPUT BUS and latch 303. However, Crater does not disclose that redundancy accumulator 301 obtains its input data from a memory of which it is configured as a cache, nor doing so in response to the block operand not being present in the accumulator. As argued above, Crater's redundancy accumulator 301 is not configured as a cache of any sort. Crater specifically discloses that data is received into accumulator 301 not from any memory, but rather that "[i]n operation, a byte from a received physical track is read into latch 303..." (col. 8, lines 56-57). Further, Crater shows in FIG. 2 and FIG. 3 that this data bus corresponds to the DEV ADT bus, which interfaces data directly from disk drive subset 103. Thus, Crater's redundancy accumulator 301 does not operate to load data from a memory of which it is configured as a cache in response to that data not being present, as recited in claim 5.

In responding to the above remarks in the Final Action, the Examiner asserts that (1) data transfers between a host processor and a redundancy group of Crater must pass through redundancy accumulator 301 and (2) the operand for redundancy calculation may come either from a disk drive or the intermediate results stored in the redundancy accumulator 301, via data selector 304, "depending on if the operand is directly available from the redundancy accumulator." The latter assertion is simply incorrect. As described at col. 8, line 56 – col. 9, line 63, redundancy accumulator 301 has two modes of operation: read and accumulate. In read and accumulate modes respectively, a logical 0 or 1 is stored into pointer memory 302 when the corresponding location of redundancy accumulator 301 is accessed. The value stored in pointer memory 302 for a particular location of redundancy accumulator 301 controls (via latch 307 and data selector 304) whether input data or input data accumulated with stored data (via redundancy calculator circuit 305) is stored within redundancy accumulator 301. This process of storing data into redundancy accumulator 301 has nothing whatsoever to do with the presence or absence of an operand within the accumulator, as required by claim 5. Rather, Crater's storing of data

depends on the mode in which the accumulator is operating. Thus, Crater fails to anticipate claim 5.

Numerous other ones of the dependent claims recite additional distinctions over what is disclosed in Crater or the other cited references. However, as the independent claims have been shown to be distinguishable, further discussion of the dependent claims is unnecessary at this time.

In light of the foregoing remarks, Applicant submits the application is in condition for allowance, and notice to that effect is respectfully requested. If any extension of time (under 37 C.F.R. § 1.136) is necessary to prevent the above referenced application from becoming abandoned, Applicant hereby petitions for such an extension. If any fees are due, the Commissioner is authorized to charge said fees to Meyertons, Hood, Kivlin, Kowert & Goetzel PC Deposit Account No. 501505/5681-05200/RCK.

Also enclosed herewith are the following items:

☒ Return Receipt Postcard

☒ Notice of Appeal

Respectfully submitted,

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